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Performance Improvement of Spacer-engineered N-type Tree Shaped NSFET towards Advanced Technology nodes

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ABSTRACT

Tree-shaped Nanosheet FETS (NSFET) is the most dependable way to scale down the gate lengths deep. This paper investigates the 12nm gate length (L_G) n-type Tree-shaped NSFET with the gate having a stack of high-*k* dielectric (HfO_2) and SiO_2 using different spacer materials, which can be done using TCAD simulations. The Tree-shaped NFET device with $T_{(NS)}$ = 5 nm, $W_{(NS)}$ = 25 nm, W_{IB} = 5 nm, and H_{IB} = 25 nm has high on-current (I_{ON}) and low off-current (I_{OFF}). The 3D device with single-*k* and dual-k spacers are compared and its DC characteristics are shown. It is noted that the dual-*k* device achieves the maximum I_{ON}/I_{OFF} ratio, which is 10^9, compared to 10^7 because the fringing fields with spacer dielectric lengthen the effective gate length. Additionally, the impact of work function, interbridge height, width, gate lengths, and temperature, along with the device's analog/RF and DC metrics, is also investigated in this paper. Even at 12 nm L_G, the proposed device exhibits good electrical properties with DIBL = 23 mV/V and SS = 62 mV/dec and switching ratio (I_{ON}/I_{OFF}) = 10^9. The device's performance confirms that Moore's law holds even for lower technology nodes, allowing for further scalability.

INDEX TERMS: Single-*k* spacer; dual-*k* spacer; Tree-shaped NSFET, Nanosheet; Spacer engineering.

I. INTRODUCTION

The electronic industry has worked continuously for the last 60 years to meet the ever-increasing demand for electronic gadgets used in many applications. This is because electronic devices perform better at every technological level in compactness, cost-effectiveness, good performance, and less power consumption [1]. The fundamental components of many electronic gadgets in today's market are the transistors, which are applied in many circuits. Because of Moore's law, it is necessary to incorporate more transistors into the single integrated circuit (IC) to support the many electronic applications [2]. Because of scaling down the device's dimensions, the conventional MOSFETs are affected by short channel effects (SCE) [3]. FinFETs have enabled the scaling of the CMOS to allow the lower technology node, maintaining Moore's law. However, when dimensions decrease below the 5-nm node, FinFETs encounter several issues. The electric field at the sidewall is always enhanced compared to the corner's electric field, decreased device performance, decreased electrostatics, and significant process variability [4] – [8].

To reduce SCEs, it is crucial to have an innovative device whose channel has more control over the gate, so the gate should surround the channel. A gate-all-around (GAA) Nanowire and Nanosheet structure with vertical channels was recently introduced to allow scaling toward sub-5-nm technological nodes [5-8]. Multiple stacked channels are present in the NW and NS structures, which can significantly enhance the on-state current and output characteristics. Additionally, NW FETs are currently regarded as one of the best substitutes for Fin-FETs due to their improved gate control. Further, due to the more control of the gate and very thin Nanowire, the SCEs in the NW FETs have significantly dropped compared to the FinFETs, whose device performance is depreciated in the lower node [9], [10]. This has improved electrostatic integrity. Regarding layout efficiency, power consumption,

and scalability in CMOS design, vertical GAA Nanowire FETs outperform FinFETs and even horizontal GAA Nanowires [11]. Several channels can be used in GAA FETs, which are silicon nanowires/nanosheets stacked vertically, to achieve the necessary performance in applications like DC, analog, and RF [12], [13].

In NW-FET, it is necessary to have a wide gap between two adjacent NWs, which poses problems in the fabrication, and the aspect ratio of the channel stack is increased. It has decreased drive currents, higher parasitics, and lesser channel widths [14]. An excellent option for effectively suppressing the short-channel effects and achieving fantastic current drivability is the Nanosheet-FET (NSFET) with gate wrapping on all four sides. [15].

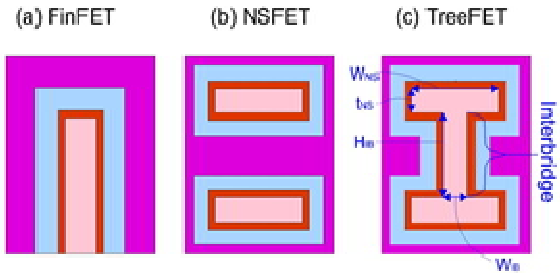


FIGURE 1. Schematic of (a) FinFET (b) NSFET (c) Tree shaped NSFET's channel cross-sections.

Additionally, NSFETs offer improved channel effective width (W_{eff}), allowing for increased current drivability in the same footprint while maintaining better electrostatics [16]-[18]. To further increase the on current, the researchers designed the FETs with different channel shapes [19] – [21]. The tree-shaped channel geometry has gained much attention in the semiconductor industry, especially among these channel shapes [22]-[24]. As shown in Fig.1, the Tree-shaped NSFET channel combines Nanosheet FET and Fin-FET. The channel is constructed by linking the two nanosheets by an inter-bridge (IB), which is in the shape of a fin to form the Tree-shaped NS-FET.

Without additional space, this inter-bridge provides an extra drive current for the vertically stacked MOSFETs [22]. However, in sub-10 nm devices, the space between the source and channel or the drain and channel is less and suffers from charge-sharing phenomena. SCEs are caused by the rise in the drain potential effect on the channel. Thus, spacers are added, increasing the gate control and the space between the source and drain to lessen the adverse effects. However, spacers raise the series resistance and have an impact on the flow of the carriers, which reduces the I_{ON}. High-k spacers, which increase I_{ON}, are presented to address this issue. However, using a high-*k* spacer introduces several problems, such as gate capacitance associated with the fringe that delays the circuit and forms the traps, which will lower the carrier mobility because of Coulomb scattering. To solve this problem, a dual-*k* spacer that combines the low-k in the outer region and high-*k* in the inner region is introduced. This work investigates the single-*k* and dual-*k* spacer effects on the Tree-shaped NS-FET.

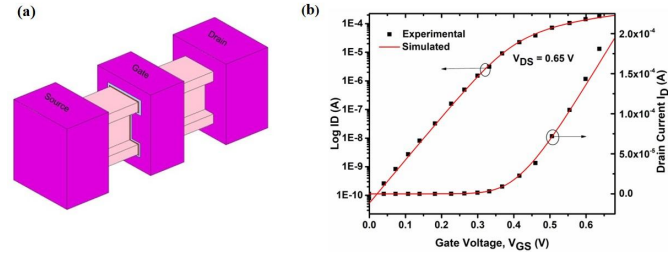
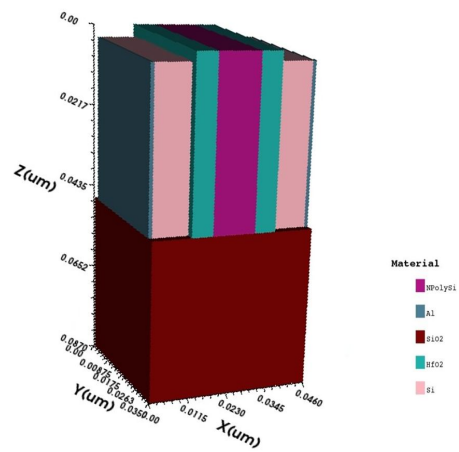


FIGURE 2. (a) 3D view of Tree-shaped NSFET (b) calibration of NSFET.

II. DEVICE STRUCTURE AND SIMULATION DETAILS:

Fig. 2(a) shows the 3-D portraits of Tree-shaped NSFET. The interbridge, which acts as a channel, is formed in the NSFET structure to increase channel conduction. The device details of Tree-shaped NSFET are shown in Table I. Gate length (L_G), width of Nanosheet W_{NS}, thickness of Nanosheet T_{NS}, width of the interbridge (W_{IB}), and height of interbridge (H_{IB}) are the critical design parameters. The main primary Tree-shaped NSFET parameters, Lg, W_{NS}, and $T_{NS,}$ are fixed at 12, 25, and 5 nm, respectively. Tree-shaped NSFET's W_{IB} and H_{IB} are 5 and 25 nm, respectively, and the channel material used is silicon, the gate oxide consists of a stack of SiO_2 and HfO_2 with the effective oxide thickness (EOT) of 0.9 nm, and the single spacer of HfO_2 is used. The gate's work function (φ_m) is 4.746 eV and the channel doping (n-type) is fixed to 10^{19} to design the Tree-shaped device. The experimental data [30] is calibrated and confirmed to correspond with the simulated data to achieve the device simulations with accuracy, as shown in Fig. 2(b). Figures 3 (a) and 3(b) show the three-dimensional view of a single and dual spacer, respectively. Fig. 3(c) and 3(d) show the two-dimensional view of single and dual spacers. Models like the Slot boom bandgap narrowing model, band-to-band auger model, and many other simulation models are also included. The detailed Tree-shaped NSFET design's fabrication flow is seen in Fig. 4.

(a)



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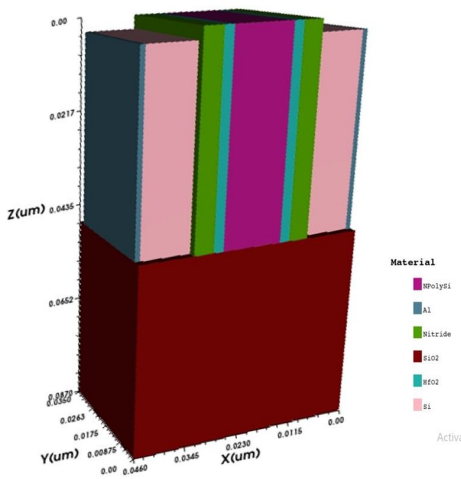
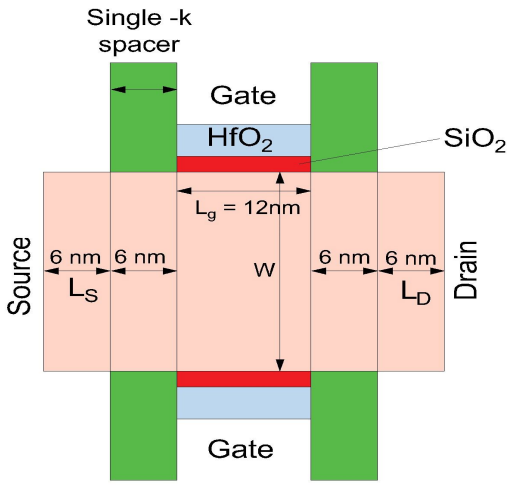


(c)



(d)

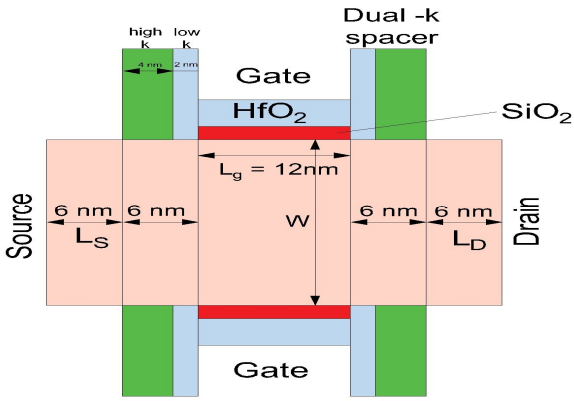


FIGURE 3. Architecture of Tree-shaped NSFET (a) 3-dimensional view of the single-k spacer, (b) 3-dimensional view of dual-k spacer, (c) 2-dimensional view with single-(k) spacer (d) 2-dimensional view with dual-(k) spacer.

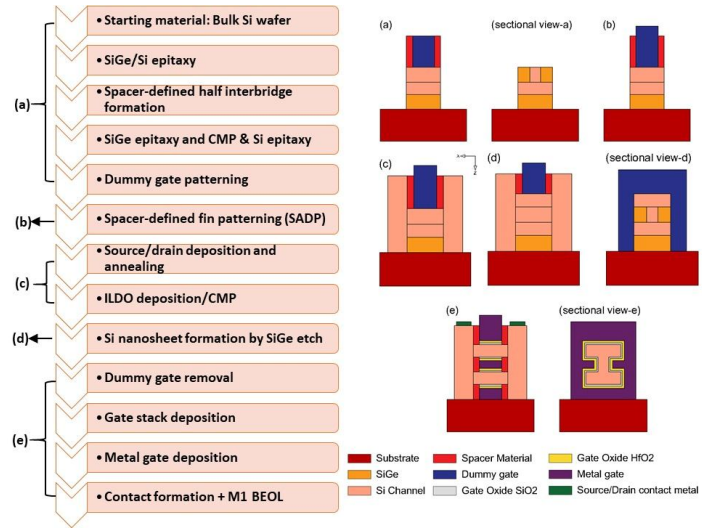


FIGURE 4. Fabrication flow of Tee-shaped NSFET.

TABLE I
DETAILS OF TREE-SHAPED NSFET

Device Parameter	*Symbol*	*TREE-SHAPED NSFET*
Length of the gate	L_G	12nm
Width of the device	$W_{(NS)}$	15-20nm
Thickness of the device	$T_{(NS)}$	3-5nm
Channel material	-	Silicon
Width of the interbridge	W_{IB}	3 – 5 nm
Height of the interbridge	H_{IB}	15 – 25 nm
Gate oxide thickness (T_{OX})	SiO_2	0.6nm
Gate high-(k) dielectric thickness	HfO_2	1.7nm
Effective Oxide Thickness	EOT	0.9nm
Gate work function	φ_m	4.76ev
Single-(k) spacer length	-	5nm
Dual-(k) spacer length	-	6nm

III. ANALYSIS OF RESLUTS:

A. ELECTRICAL CHARACTERISTICS OF TREE-SHAPED NSFET:

This section shows the electrical properties of Tree-shaped NSFET and NSFET at the following dimensions: L_G = 12 nm, $T_{(NS)}$ = 5 nm, $W_{(NS)}$ = 20 nm, H_{IB} = 15 nm, W_{IB} = 3 nm. Fig. 5 displays the Id –Vg characteristics of Tree-shaped NSFET and NSFET. At V_{GS} = 0.7 V and V_{DS} = 0.7 V, Tree-shaped NSFET has an on current I_D of 2.4 x 10^{-5}A, OFF current I_{OFF} of 1.12 x10^{-14} A, and NSFET has an on current I_D of 1.78 x 10^{-5}A and OFF current I_{OFF} of 1.20 x10^{-14} A. The Tree-shaped NSFET exhibits a higher drive current than the NSFET and almost same off current. The I_{on}/I_{off} ratio increases by 33% from NSFET to Tree-shaped NSFET.

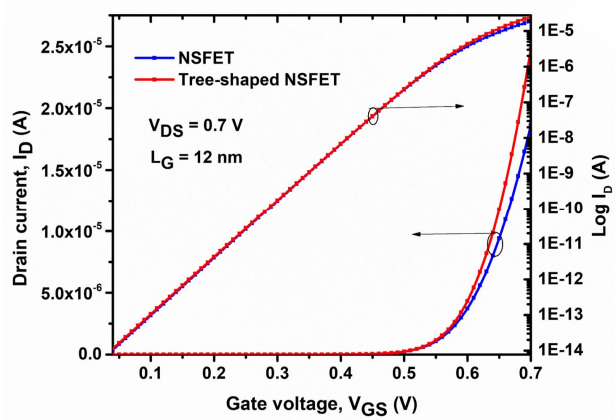


FIGURE 5. I_D VS V_{GS} characteristics of NSFET and Tree-shaped NSFET.

The I_D vs V_{GS} and I_D vs V_{DS} for different V_{DS} and V_{GS} are shown in Figures 6(a) and 6(b). Transconductance assesses the device's potential for high-speed circuits. Fig.6(c) displays the quantified change in drain current with a change in the gate voltage, and the expression is given as $g_m=I_D/V_{GS}$. The g_m for the Tree-shaped NSFET is 3 x10^{-4} S. To accommodate applications like high frequency, the gm peak has to be high at the bias point. The amount of transconductance that can be obtained for each amp of output current is identified as the transconductance generation factor (TGF = g_m/I_D). A higher TGF value ensures reduced maximum power dissipation in capacitive load circuits and improved input drivability. A higher TGF value ensures reduced maximum power dissipation in capacitive load circuits and improved input drivability. The TGF obtained for the Tree-shaped NSFET is around 45 V^{-1}as shown in Fig.6 (d). Fig.6 (e) shows the output conductance, which shows the change in drain current with the change in Drain voltage V_{DS} at a V_{GS} = 0.7 V. A lower g_{ds} is advantageous as it means that the channel control by the drain reduces and lessens the channel length modulation effects, which guarantees the device's suitability for the applications like a constant current source. The saturation region is used for operating the devices in analog circuits. Usually, I_D operates in the saturation area independent of V_{DS}. However, because of short-channel behavior, V_{DS}'s impact on channel electrostatics leads I_D to vary. Thus, output conductance g_{ds} is analyzed to determine how much I_D impacts due to V_{DS}. The device exhibits decent g_{ds}.

Additionally, as seen in Fig. 6(f), an increase in gm enhances the intrinsic gain of NSFET, which is an important metric for analog circuits. Tree-shaped NSFET has a very good intrinsic gain. Without any parasites, the intrinsic capacitance is the gate to oxide capacitance (C_{ox}). Any device's power consumption and dynamic power are determined using the C_{ox}. Fig. 6(g) illustrates the intrinsic capacitance. A crucial parameter for assessing a device's viability for radio frequency applications is the C_{gg}, whose fluctuation with V_{GS} is shown in Fig. 6(h). The sum of the C_{gs} and C_{gd} is the total gate capacitance (C_{gg}). The Gain Bandwidth can be evaluated from the below equation (1), and GBW changes with V_{GS} are shown in Fig. 7(a).

$$GBW \approx \frac{g_m}{2\Pi 10(C_{gd})} \quad (1)$$

The device effectiveness for the RF application is greatly influenced by the cutoff frequency (f_T). The cutoff frequency can be evaluated from the below equation (2).

$$f_T \approx \frac{g_m}{2\Pi(C_{gd}+C_{gs})} \quad (2)$$

The cutoff frequency value is very good for Tree-shaped NSFET as displayed in Fig.7(b), making it more appropriate for RF applications. This is because there has been a substantial increase in g_m than the decrease in C_{gg}. The Gain Frequency Product is illustrated in the Fig 7(c).
The two main parameters used to assess the short-channel nature of the nano regime are SS and DIBL, which can be obtained using equations 3 and 4.

$$DIBL(mV/V) = \left|\frac{V_{th1}-V_{th2}}{V_{DS1}-V_{DS2}}\right| \quad (3)$$

$$SS = \left[\frac{\partial \log_{10} I_D}{\partial V_{GS}}\right]^{-1} \quad (4)$$

The device has a very decent subthreshold swing which is 62.9 mV/dec, and a good drain-induced barrier lowering (DIBL), which is advantageous; the Tree-shaped NSFET exhibits excellent performance. Because there is more tunnel space between the source and channel areas, the I_{ON} performs better in Tree-shaped NSFET [29]. The stacked nanosheets are separated by an interbridge (IB), which acts as a channel that facilitates a larger flow of electrons in that region. The tree-shaped NSFET was found to have a higher $I_{ON/OFF}$ ratio. Because Tree-shaped NSFET has an $I_{ON/OFF}$ ratio greater than 10^9, it can be utilized in many applications like digital circuits. The equation 5 represents the proposed device's effective width (W_{eff}) [29].

$$W_{eff} = 2n(W_{NS} + T_{NS}) + 2(H_{IB} - W_{IB}) \quad (5)$$

Where n, in this case 2, is the number of NSs. Furthermore, the influence of spacers like single-(k) and dual-(k) on the characteristics of Tree-shaped NSFET are also explored in this paper.

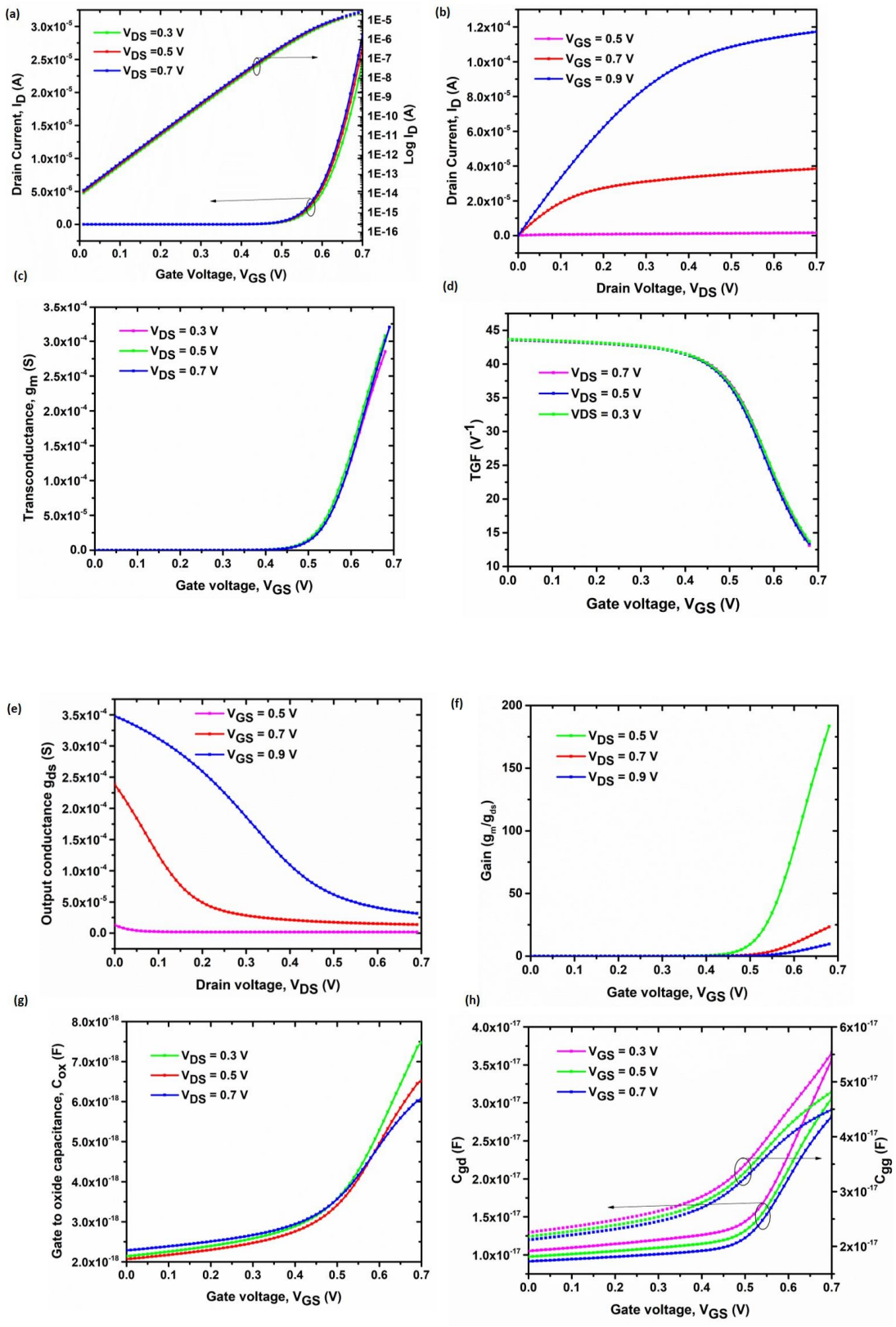


FIGURE 6. **(a) The transfer characteristics (I_D-V_{GS}) of device at V_{DS} = 0.7 V (b) output characteristics (I_D–V_{DS}) (c) Transconductance (g_m) (d) Transconductance generation factor (TGF) (e) output conductance (g_{ds}) (f) intrinsic gain (g) C_{ox} (h) C_{gd} and C_{gg}.**

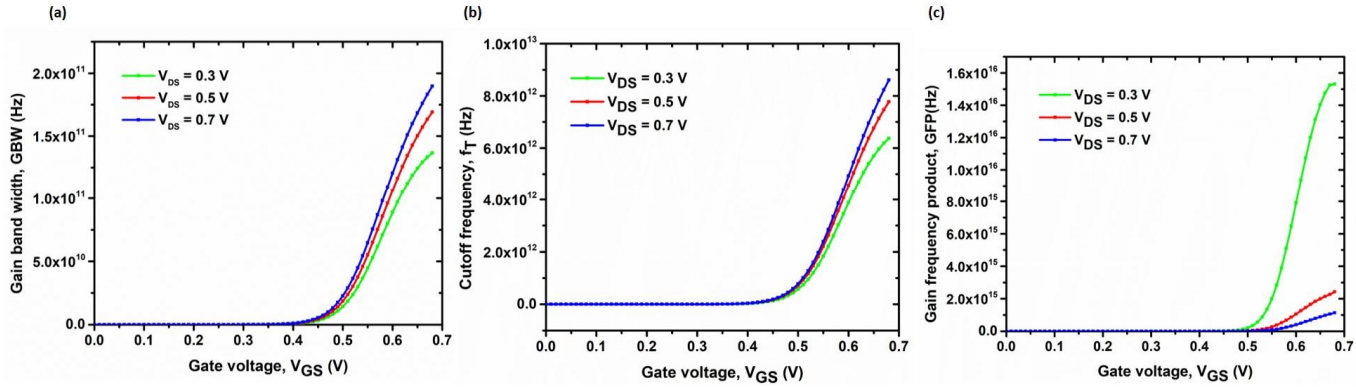


FIGURE 7. (a) Gain Band Width Product (GBW) (b) Cut-off Frequency (f_T) (C) Gain Frequency Product (GFP)

B. EFFECT OF SPACER MATERIALS ON TREE-SHAPED NSFET:

The study includes various materials for spacers with various dielectric constants (k) to examine the effect on device performance. The dielectric constant (k) of different single-(k) spacer materials Air, SiO_2, Si_3N_4, and HfO2 are 1,3,5,4.9 and 25, respectively. The single-(k) spacer effect is depicted in Fig. 8(a), and the dual-(k) spacer is shown in Fig.8(b), which indicates that a rise in the spacer dielectric the leakage current is reduced; usually leakage current is influenced by the electric field across the gate oxide. Increasing the spacer dielectric value can enhance the vertical electric field in the off-state. A higher electric field helps to control the depletion region better, reducing the probability of carriers (electrons or holes) tunneling through the gate oxide. As a result, sub-threshold leakage current tends to decrease. As the spacer dielectric value grows, the drive current (I_D) remains nearly constant However, low-(k) decreasing performance and employing only high-(k) will lead to many problems, including formations of the traps and delay of the circuits due to fringe capacitance and will limit the mobility of the carriers. To address the aforementioned problems, a high-(k) spacer is added in the restricted area close to the gate region where the density of the carriers will be high, and a low-(k) spacer is introduced in the area left to reduce I_{OFF}. As a result, dual-(k) spacers are used. The combinations of Air and HfO_2, SiO_2 and HfO_2, Si_3N_4, and Air, which are hybrid, and Si_3N_4 and HfO_2 are evaluated in this paper. Table II shows that important metrics like I_{ON}, I_{OFF}, $I_{ON/OFF}$, SS, and DIBL greatly improve as the spacer dielectric value increases. For any spacer combination at L_G = 12 nm, the device displays an $I_{ON/OFF}$ ratio of more than 10^8, which is suitable for all logic applications. The lowest SS of around 62 mV/dec with dual-(k) (Si_3N_4 + HfO_2) and (SiO_2 +HfO_2) spacer is possible at 12 nm nanostructure. The HfO_2 beats other single-(k) spacers in successfully managing SCEs and achieves the highest I_{ON}/I_{OFF} ratio. Furthermore, the dual(k) spacers Si_3N_4 + HfO_2 and SiO_2 + HfO_2 exhibit higher performance in dual-(k) spacers with a 10^9 I_{ON}/I_{OFF} ratio, lower I_{OFF}, and basic scaling benefit. The enlargement of fringing fields through the use of spacers is deliberately employed to reduce parasitic bipolar junction transistor (BJT) action and, consequently, lower off-state current, Digital performance is improved by effective use of the high-(k) (HfO_2) at the inner region in the dual-(k) (Si_3N_4+ HfO_2) and (SiO_2+ HfO_2) spacer. Additionally, the dual-(k) (Si_3N_4 + HfO_2) spacer reduces direct source to drain tunneling, improving switching (I_{ON}/I_{OFF}) and many electrical characteristics at lower technology nodes. To determine the drive current deterioration brought on by trap-assisted recombination, the SRH model incorporates deep-level faults.

Moreover, unlike other dielectric materials, TiO_2 suffers from various traps. For this reason, TiO_2 has not been used in experiments as a gate dielectric. High electric field devices lower device dependability. In nanoscale geometric devices, the electric field is typically stronger toward the drain side, which causes the electrons to reach higher energies, known as hot carriers. The impact ionization that these hot carriers produce close to the drain terminal leads to a drain-to-body current. Nonetheless, the suggested device's SOI structure and spacer gap between the drain and gate potential terminals guarantee decreased hot carrier effects, electric field, and leakage currents in the off-state.

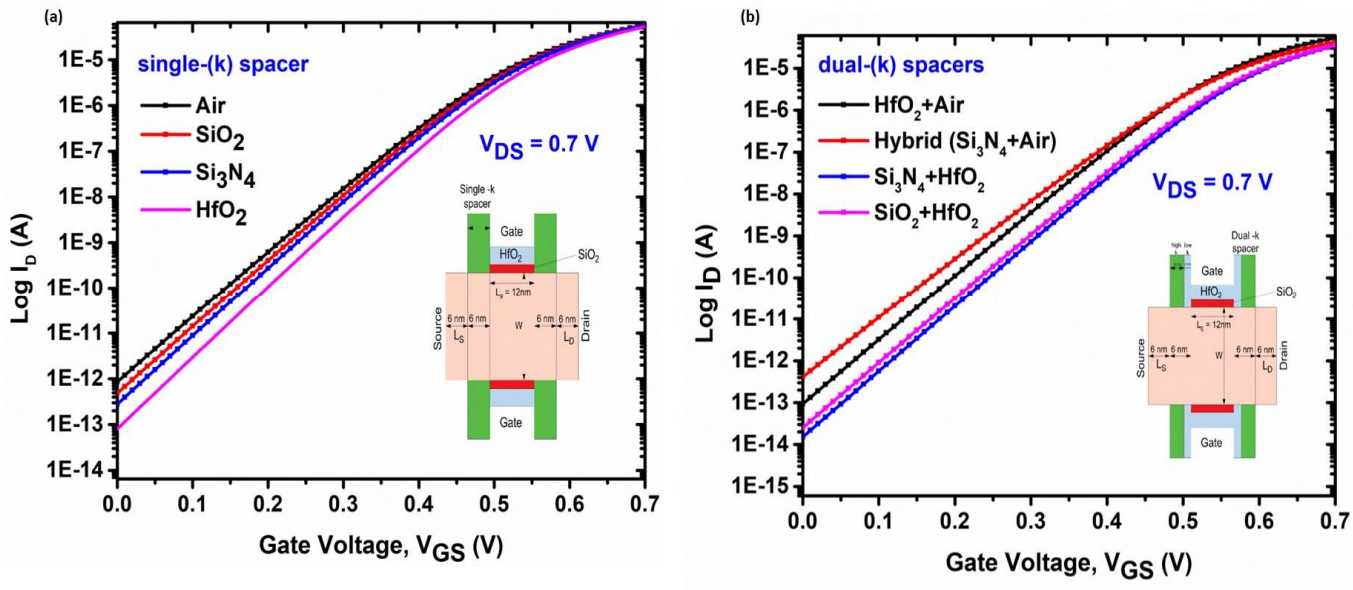


FIGURE 8. **Effect of (a) single-(k) spacer (b) dual-(k) spacer of Tree shaped-NSFET.**

TABLE II
ELECTRICAL CHARACTERISTICS OF SINGLE-(K) AND DUAL-(K) SPACERS

Single-(k)/dual-(k) spacers	*V_{th} at V_{DS}=0.7V*	*Vth at V_{DS}= 0.05V*	*DIBL (mV/V)*	*SS (mV/dec)*	*I_{ON} (A)*	*I_{OFF}(A)*	*$I_{ON/OFF}$*
Single-(k)							
Air	0.304	0.312	74	69.5	3.68×10^{-5}	5.31×10^{-13}	8.5×10^{7}
SiO_2	0.298	0.340	65.9	67.7	3.60×10^{-5}	3.04×10^{-13}	3.40×10^{8}
Si_3N_4	0.312	0.353	58.16	66.4	3.68×10^{-5}	1.01×10^{-13}	3.64×10^{8}
HfO_2	0.370	0.391	41	63	3.69×10^{-5}	1.09×10^{-14}	3.3×10^{9}
Dual-(k)							
Air + HfO_2	0.33	0.35	33	65	4.01×10^{-5}	9.26×10^{-14}	4.33×10^{8}
Hybrid (Si_3N_4 +Air)	0.349	0.351	52	67	3.86×10^{-5}	4.11×10^{-13}	9.39×10^{7}
SiO_2 + HfO_2	0.371	0.387	23	62.1	3.01×10^{-5}	9.80×10^{-15}	3.07×10^{9}
Si_3N_4+ HfO_2	0.382	0.391	38	63	3.24×10^{-5}	8.90×10^{-15}	3.64×10^{9}

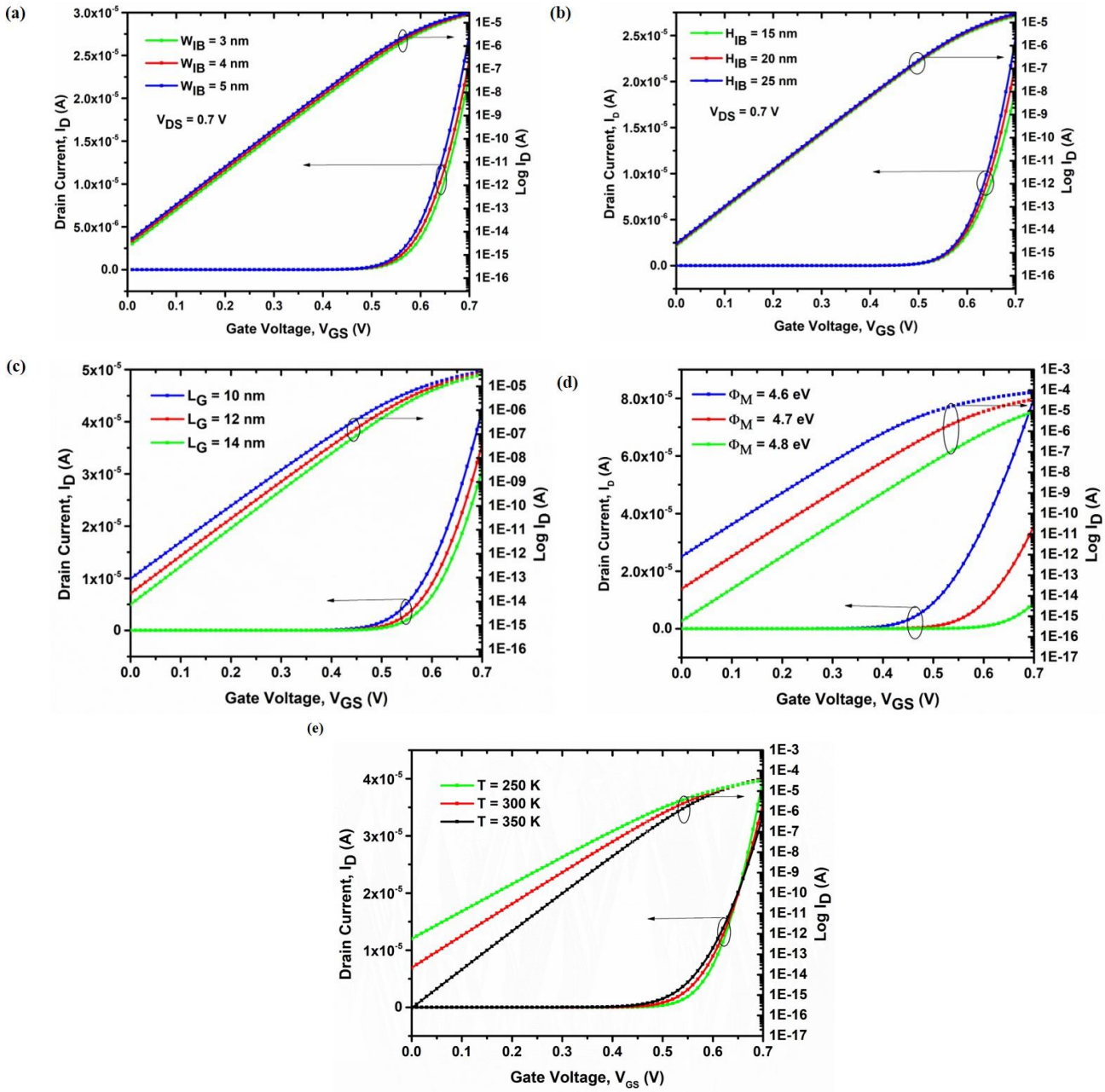


FIGURE 9. I_D-V_{GS} graph with various (a) interbridge widths (WIB) (b) interbridge heights (HIB) (c) Gate lengths (L_G), (d) work function (e) Temperatures.

C. EFFECT OF SCALING, TEMPERATURE AND WORK FUNCTION:

The impact of IB width (W_{IB}) on tree-shaped NSFET is discussed in this subsection. Fig.9 (a) illustrates the interbridge width variation with W_{IB}= 3-5 nm in steps of 1 nm at L_G = 12 nm and height of interbridge H_{IB} = 25 nm and it shows the I_D -V_{GS} characteristics for various W_{IB}. It is noticed that when the W_{IB} rises, the drain current (I_D) rises monotonically as a result of the rise in the device's effective width (W_{eff}). As we increase W_{IB} from 3 to 5 nm, I_{ON} is seen to improve by a good percentage. In addition, the leakage currents increase as the width of the interbridge (W_{IB}) increases. As the interbridge width increases, the rise in leakage currents will cause the device's OFF currents to grow, resulting in a high I_{OFF}.

The impact of IB height (H_{IB}) on Tree-shaped NSFET is discussed in this subsection. Fig.9 (b) illustrates the interbridge height variation for tree-shaped NSFET with H_{IB}= 15 – 25 nm in steps of 5 nm at L_G = 12 nm and width of interbridge W_{IB} = 5 nm. Compared to H_{IB} = 15 and 20 nm, H_{IB} = 25 nm provides a greater drive current. The tunneling area has grown, raising the effective width (*Weff*) and boosting the drive current. As H_{IB} increases from 15 to 25 nm, I_{ON} is seen to improve.

The L_G fluctuation at V_{DS} = 0.7 V and V_{GS} = 0.7 V is shown in Fig.9(c). As L_G increases, the control of the gate

becomes more effective and reduces the leakage current. Due to the decrease in gate length L_G, the SCEs rise because of the various effects like charge sharing, so the I_{OFF} rises due to decreased gate power through the channel.

As shown in Fig.9 (d), a rise in the work function causes the leakage current (I_{OFF}) to decrease significantly and the I_{ON} to drop considerably. Increased gate work function ensures better performance of the device when the device is in the off state. Additionally, a rise in the electron tunneling barrier causes a decrease in the gate-to-source and gate-to-drain extension tunneling in the off-state and a reduction in the gate-to-channel tunneling with the rise in work function [31]. In addition, overall performance of the device increased [34], [35]. According to Fig.9 (e), as temperature rises, I_{OFF} rises as well, while I_{ON} varies only slightly. Diffusion current and SRH recombination, two temperature-dependent processes, are responsible for a rise in I_{OFF} with rising temperatures.

TABLE V
COMPARISON OF PROPOSED RESULTS WITH EXISTING RESULTS

Device	*LG*	*Work Function (eV)*	*EOT (nm)/oxide thickness*	*SS (mV/dec)*	*ION/OFF*
NSFET[32]	16nm	4.456	0.78nm	62.2	3.30×10^7
JL-NSFET[33]	16nm	4.8	0.7nm	76	1.94×10^7
Dual(k) Tree shaped NSFET[proposed]	12nm	4.76	0.9nm	62.1	3.64×10^9

IV. CONCLUSION

This study examines Tree-shaped NSFET with a 12 nm gate length that can scale beyond to assess the digital and analog/RF performance parameters. The I_{ON}/I_{OFF} ratio is high in the proposed Tree-shaped NSFET, making it acceptable for digital applications. The proposed tree-shaped NSFET has better I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, transconductance gm, output conductance g_{ds}, and cut off Frequency f_T. This paper also analyses the influence of single-(k) and dual-(k) spacers on Tree shaped NSFET. Due to the limited high-(k) usage in the surrounding area of the gate region and the low-(k) in the remaining portion, the spacer with dual-(k) materials performs better than any other spacer dielectric materials at 12 nm gate length. The dual-(k) spacer SiO_2+HfO_2 and Si_3N_4+HfO_2 surpass all previous spacer dielectrics.

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