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Spacer Dielectric Analysis of Multi-Channel Nanosheet FET for Nanoscale Applications

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ABSTRACT This work investigates the effect of single and dual-*k* spacer materials consisting of different dielectric constants (*k*) in optimized nano-channel gate-stack nanosheet (NS-FET) employing hafnium oxide and silicon dioxide as gate insulator to improve its sub-threshold performance. The effect of the external low-k spacer modification in the dual-k spacer has been shown by adjusting the inner high-k spacer. The drain-induced barrier lowering (DIBL) in this modification with dual-k spacer is 14 mV/V, which is a significant improvement above single spacer NS-FET. The Visual TCAD 3D Cogenda tool is used to examine the performance of the developed NS-FET with air, single, dual-k, and hybrid spacers. The CADENCE platform is used to perform circuit aspects. Additionally, a comparison of the device architecture's performance study with respect to DC characteristics is made. DC parameters of the proposed device are established: I_{ON} to I_{OFF} ratio of approximately 10^5, DIBL of approximately 14 mV/V, sub-threshold swing (SS) of approximately 62 mV/dec, and low threshold voltage (Vth) of 0.38 V. The analysis on power consumption for advanced NS-FET is also analyzed with single-*k* and dual-*k* spacers. The performance of single-*k* and dual-*k* spacer dielectric variation for CMOS inverter is also shown. Furthermore, low power consumption by this NS-FET ensures improved device performance suitable for nanoscale semiconductor industries.

INDEX TERMS CMOS Inverter, DIBL, Dielectric Material, Gate-all-round (GAA), Power Consumption, Nanosheet (NS) FET, Silicon on Insulator (SOI).

I. INTRODUCTION

According to technical advancements, when an electronic gadget gets smaller, its complexity rises, and its performance improves. The development of transistors towards nanometer technology has improved its working performance while maintaining the benefit of mobility at smaller dimensions. As per the International Road map for Devices and Systems (IRDS), devices close to the nanometer range are most appropriate for low-power as well as high frequency applications [1].

The FinFETs have developed vastly during the past decade as transistor size has drastically decreased. Considering their height/width ratio, FinFETs may operate efficiently on nanometer technologies ranging from below 32 nm to 10 nm [2]. FinFET is a multigate device that uses dual or multi-gates wrapped around the channel on a substrate to reduce short-channel effects (SCE) and provide better control on an electrostatic channel. FinFETs are particularly suitable for low-power integrated circuits. Furthermore, FinFETs demonstrate a notable proficiency in promoting vertical tunneling as opposed to corner tunneling. This achievement is attributed to the integration of a vertical-tunnel FET designed with negative capacitance. Since of its creative design, the transistor switch operates more efficiently since it creates a powerful vertical electric field [3].

Tri-gate construction is used to enclose all the three sides of the channel. FinFETs still have a variety of design, device performance, structural, and cost-effectiveness

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issues that hinder further scaling down despite this advancement [4]. Fin architectures must be able to maintain optimal performance even when device dimensions are reduced. Furthermore, SCEs can be restricted by having a robust channel control structure regulating the channel from all directions, which is essential for technology nodes smaller than 10 nm.

The potential of gate-all-around (GAA) NS-FET is greater when compared to current FinFET technology due to better gate controllability [5]. While scaling is continuous, the gate is enclosed by the channel from all sides. The most suitable alternatives to update FinFET in the sub-10-nm zone are GAA devices like nanowires and nano-sheets. SOI technology involves an insulator substrate like SiO_2 (silicon dioxide) being coated by a thin layer of active region [6]. FDSOI technology is best used in enhanced versions of next-generation wireless applications operating at high frequency and low power [7]. Junctionless transistors (JLTs) can be designed with nano-sheet devices in mind by guaranteeing consistent doping in the channel material, which prevents the formation of junctions between the drain/source and channel [8]. Eunseon *et. al.* highlighted that adopting inverted-T Bulk FinFET technology has various benefits, including lower wafer costs, reduced occurrence of defects, and ineffective change in thermal energy [9]. However, there may be an issue with the substrate leaking hindrance. By combining two gate insulators above an un-doped substrate, gate-stack technology may significantly reduce leakage. Chiang *et. al.* inferred that the investigations on JLT technology can boost the ON current (I_{ON}) as it has a larger channel volume, broader width of the Fin, and low thickness [10].

The single, dual, or GAA FET, lightly doped drain (LDD) implantation, designed gate, or bulk FET are employed in the existing literature. Every method that has been developed has improved switching times between devices or SS. The authors of this work tackled the difficulties by designing a Junction-less NS gate-stack SOI FinFET and evaluating its performance on spacer regions using a variety of dielectric materials, highlighting the shortcomings of current technologies in terms of practicality and dependability.

The proposed device structure, physical model description, simulation result calibration, and possible fabrication steps to realize the device are explained in section II. The DC analysis results are demonstrated and the physics behind it are discussed in section III. The power analysis and circuit performance are presented in section IV and section V respectively. Finally, concluding remarks on the manuscript are given in Section VI.

II. DEVICE STRUCTURES AND SIMULATION METHOD

The three-dimensional (3D) device structure of the NS-FET is based on 10 nm technology node [11]-[14]. Fig. 1 depicts the front and side view of the device wherein the NS-FET is designed with gate length, fin width, and channel height of 10 nm each. NS-FET is designed to have two channels with 15 nm channel spacing on both sides. The device parameters are presented in Table I.

The FinFET is implemented with two evenly doped channels with donor doping concentrations of 10^{18} cm^{-3}. Both Source and Drain have a consistent donor doping level of 10^{20} cm^{-3}. The Gate contact is made of polysilicon with a work function of 4.5 eV. HfO_2 and SiO_2 are used to make the FinFET gate oxide [6], [15]. As the dimensions of transistors shrink, the gate oxide thickness also needs to decrease to maintain proper control over the channel. The trend of reducing the gate oxide thickness in traditional SiO_2-based devices increases gate leakage and power consumption. High-*k* dielectric material is used for this purpose along with SiO_2. The channel is insulated using low- and high-*k* materials with a total thickness of 2 nm. This inhibits the gate current from evading into the channel and ensures insulator sealing. The device functions more efficiently when a dielectric material is placed in between the channel's source and drain [11].

The source and drain are directly connected to the gate for creating an NS-FET, as shown in Fig. 1. Insulators are used in the spacing area to reduce parasitic capacitance, which increases resistance. To achieve this, single and dual dielectric spacer materials are used to fill the region created between the gate and source/drain [16-18]. These regions contribute to reducing SCE and improving device performance. The spacing area can be deposited with a low *k* dielectric material like air and SiO_2 as shown in Fig. 1(a) and 1(b). The dual-spacer arrangement of high and low dielectric materials in the spacer region can be observed in Fig. 1(c) and 1(d). The length and width of each side are 15 nm and 20 nm respectively in a single spacer arrangement. In the dual spacer case, a high-*k*, and low-*k* insulator combination of length 5 nm adjacent to the gate and 10 nm adjacent to the source/drain region are considered respectively with a width of 20 nm [19]. The Cogenda Visual TCAD device simulator was used to simulate these devices [20]. The Lombardi mobility model, Shockley-Read-Hall (SRH), and Auger recombination models are all used in the simulation to represent minority carrier recombination. Additionally, the simulation uses the QDDM model from Visual TCAD, which will consider the quantum effects at lower nodes.

The physical models are determined upon calibration of simulation results obtained from transfer characteristics with experimental results [14]. The calibrated transfer characteristics obtained by normalizing I_{DS} with W_{fin} are demonstrated in Fig. 2, demonstrating an excellent match and justifies the consideration of appropriate physical models during TCAD simulation.

TABLE I
10 NM TECHNOLOGY: NS-FET AND FINFET DIMENSIONS

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Region	Dimension	
	NS-FET designed in this work	Fin FET considered for comparison [11]
Gate length	10 nm	10 nm
Gate Oxide thickness (High-*k*)	1 nm	3 nm
Gate Oxide thickness (Low-*k*)	1 nm	0.5 nm
Spacing Oxide (Low-*k*)	10 nm	7 nm
Spacing Oxide (High-*k*)	5 nm	2 nm
EOT	0.75 nm	0.75 nm
S/D doping concentration	$1x10^{20}$ /cm^3	$1x10^{19}$ /cm^3
Fin Pitch	20 nm	-
Channel height	10 nm	30 nm
Channel width	30 nm	10 nm
Work function	4.5eV	4.8eV
BOX	45 nm	50 nm

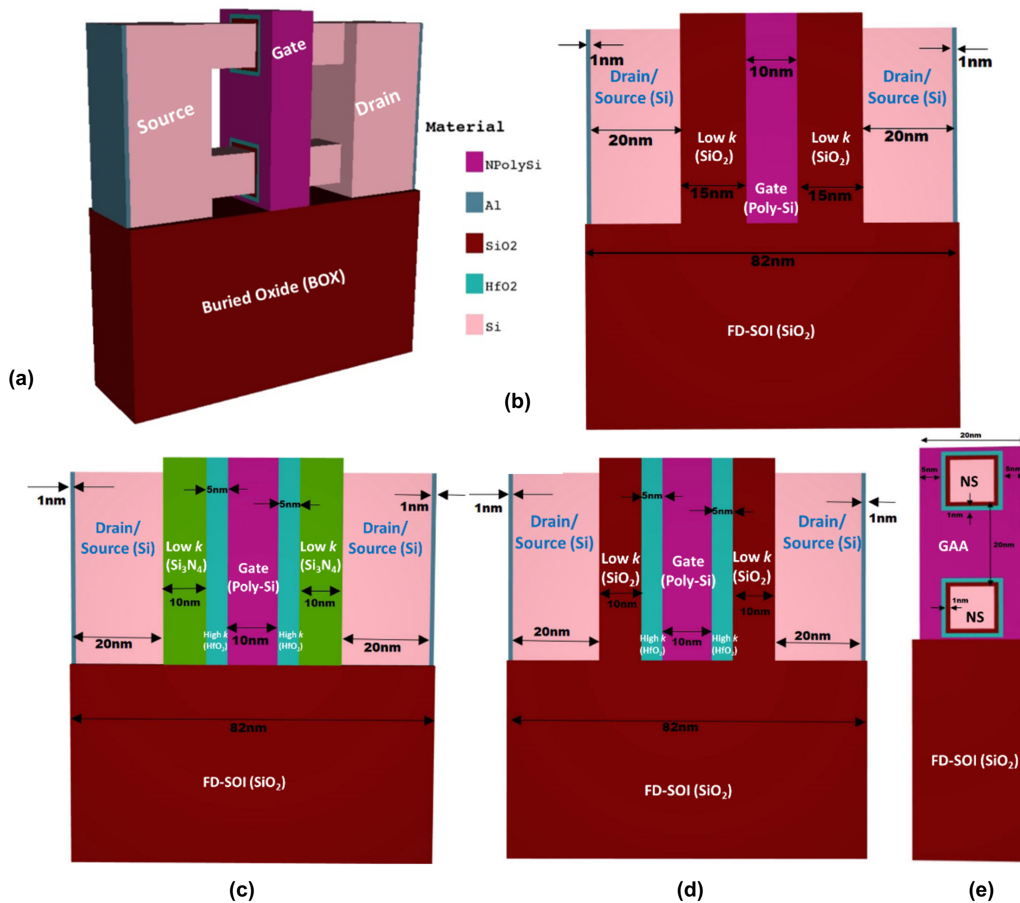

FIGURE 1. Front view of 10 nm NS-FET structure with (a) air (b) SiO_2 (c) Nitride+HfO_2 (d) HfO_2+SiO_2 spacer material (e) Side view of proposed NS-FET structure.

III. RESULTS AND DISCUSSION

The global temperature of operation of NS-FET is set at 300K. Fig. 4 shows the distribution of surface potential of the devised NS-FET at V_{GS} = 0.7V, V_{DS} = 0.75V, and doping of 10^{18} cm^{-3}. The application of V_{DS} left little potential in the channel and source regions while producing a highly concentrated potential on the drain side. The source and drain areas of the NS-FET donor distributions are heavily doped.

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The channel region is also doped with donor dopant, as shown in Fig. 4.

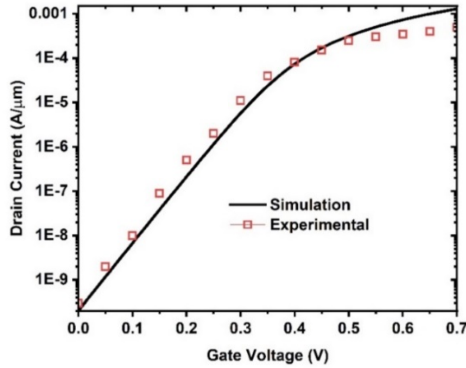

FIGURE 2. Calibration of simulated transfer characteristics with Experimental results [14].

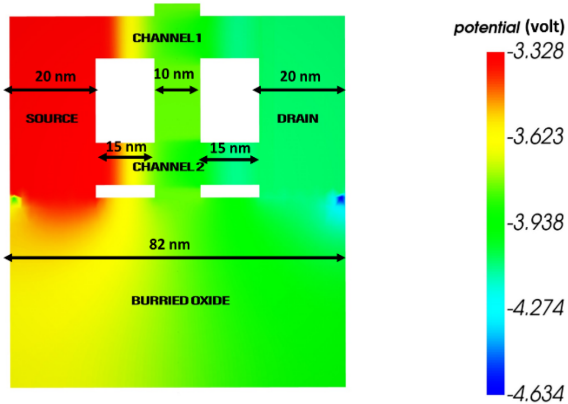

FIGURE 3. Potential distribution/ Potential difference of NS-FET at V_{GS} = 0.7V, V_{DS} = 0.75V.

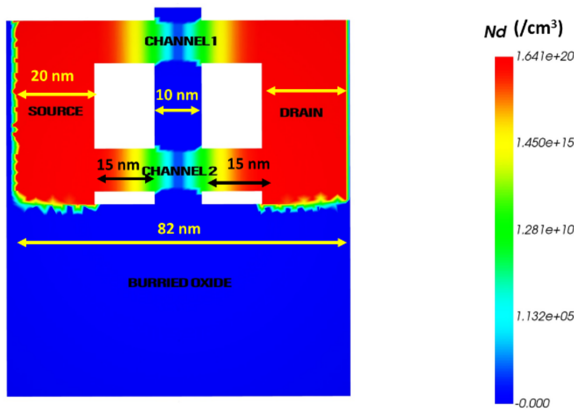

FIGURE 4. Doping Concentration (N_d) of Two-channel NS-FET.

The drain current is considered in Fig. 5 to illustrate the transfer characteristics in linear and logarithmic scales. For estimating the device's performance, the calculation of variables such as V_{th}, I_{ON}/I_{OFF} ratio, SS, and DIBL are crucial. For air, SiO_2, HfO_2+SiO_2, and HfO_2+nitride, the transfer characteristics are demonstrated. A crucial metric for evaluating the electrical performance of FET devices is the ratio of I_{ON} to I_{OFF}. The I_{ON} stands for the ON-state current and measures the device's ability to handle power when the FET is turned on. The I_{OFF}, on the other hand, depicts off-state current and shows how well FETs work to block current while it is in OFF condition. The on current, off current, and their ratio can be used to determine the switching characteristics and power efficiency of the device [3]. The ON and OFF currents and their ratio for the 10 nm NS-FET and FinFET technologies are shown and compared in Tables II and III, respectively. The values listed here represent different dielectric materials utilized to fill the voids.

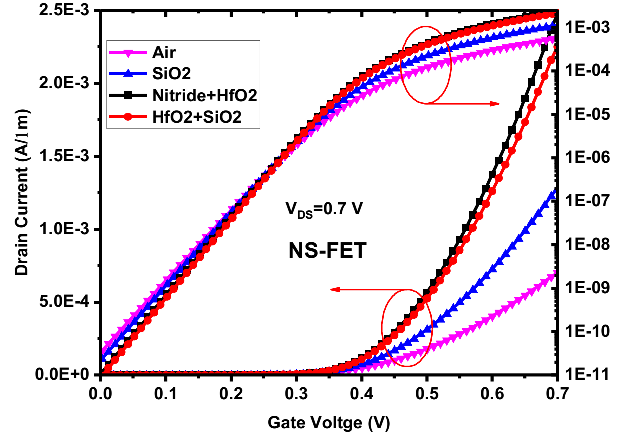

FIGURE 5. Transfer characteristics of the proposed NS-FET with single-*k* and dual-*k* spaces in linear and logarithmic scale.

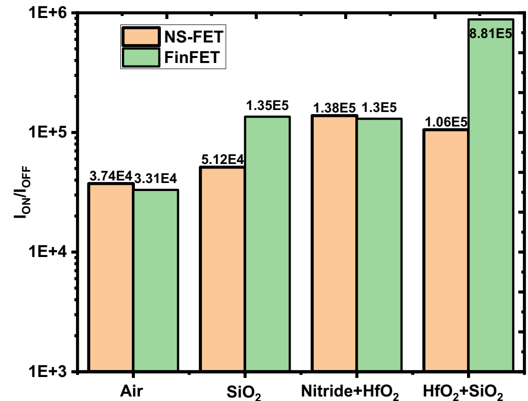

FIGURE 6. The Comparison of I_{ON}/I_{OFF} ratio for the NS-FET and FinFET with single-*k* and dual-*k* spacers.

TABLE II
ON AND OFF CURRENT ANALYSIS FOR VARYING SPACER MATERIALS: NS-FET TECHNOLOGY

Spacer Material	NS-FET I_{ON}/I_{OFF} Ratio	NS-FET I_{ON} current (A)	NS-FET I_{OFF} current (A)
Air	3.74E+04	1.11E-07	2.97E-12
SiO_2	5.12E+04	1.04E-07	2.03E-12
Nitride+HfO_2	1.38E+05	1.27E-07	0.919E-12
HfO_2+SiO_2	1.06E+05	1.15E-07	1.09E-12

TABLE III

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ON AND OFF CURRENT ANALYSIS FOR VARYING SPACER MATERIALS: FINFET TECHNOLOGY [11]

Spacer Material	FinFET I_{ON}/I_{OFF} Ratio	FinFET I_{ON} current (A)	FinFET I_{OFF} current (A)
Air	3.31E+04	8.08E-5	2.44E-9
SiO_2	1.35E+05	8.10E-5	5.98E-10
Nitride+HfO_2	1.30E+04	8.13E-5	6.24E-10
HfO_2+SiO_2	8.81E+05	8.14E-5	9.24E-11

All the NS-FETs with different spacers have I_{ON} and I_{OFF} currents in the range of 10^{-7} and 10^{-12}, respectively. FinFETs with different spacers have I_{ON} and I_{OFF} currents ranging from 10^{-5} to 10^{-11}. In contrast, NS-FET for single-k spacer outperforms FinFET regarding I_{ON}/I_{OFF} ratio calculation, improving by 10.55% for air and 73.5% for SiO_2. Fig. 6 compares I_{ON}/I_{OFF} ratio for the NS-FET and FinFET with single-k and dual-k spacers.

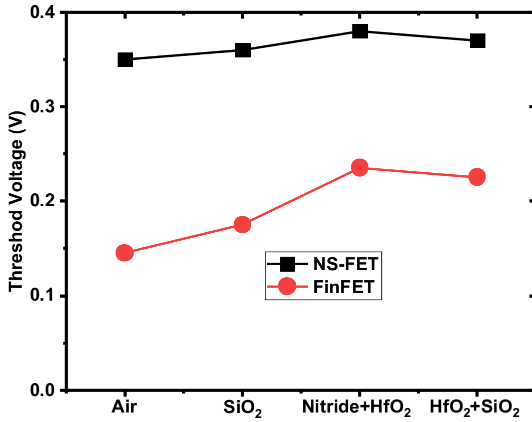

FIGURE 7. The threshold voltage of 10 nm node NS-FET and FinFET with different spacers.

It is necessary to decrease the V_{th} of NS devices to maintain satisfactory performance. It has been demonstrated that the NS-FET device can operate at a lower gate voltage by lowering V_{th}. As a result, the gate oxide layer experiences less electrical stress. This not only leads to lower power consumption but also improves the switching speed of the device [21]. Fig. 7, along with Table IV, demonstrates the threshold voltage for NS-FET and FinFET devices using single and dual-*k* dielectric materials.

The DIBL and SS are crucial short-channel parameters that determine the performance of devices. In these devices, drain potential has a significant influence on the energy band diagram in the channel region [18]. The drain bias unintentionally lowers the barrier between the source and drain, resulting in a subthreshold current, and the effect is commonly referred to as DIBL. DIBL and SS can be expressed through (1) and (2) respectively [2]. Table V depicts the DIBL values of NS-FET and FinFET for various spacer materials.

$$DIBL\ (mV/V) = \left|\frac{V_{th1}-V_{th2}}{V_{DS1}-V_{DS2}}\right| \qquad (1)$$

$$SS\ (mV/dec) = \left[\frac{\partial log_{10}(I_{DS})}{\partial V_{gs}}\right]^{-1} \qquad (2)$$

TABLE IV
THRESHOLD VOLTAGE FOR NS-FET AND FINFET FOR VARYING SPACER MATERIALS

Spaces Material	NS-FET (V_{th}) in volts	FinFET (V_{th}) in volts
Air	0.35	0.145
SiO_2	0.36	0.175
Nitride+HfO_2	0.38	0.235
HfO_2+SiO_2	0.37	0.225

TABLE V
DIBL FOR NS-FET AND FINFET WITH VARYING SPACER MATERIALS

Spaces Material	NS-FET DIBL (mV/V)	FinFET DIBL (mV/V) [11]
Air	42	121.1
SiO_2	40	98.48
Nitride+HfO_2	14	75.75
HfO_2+SiO_2	14	83.33

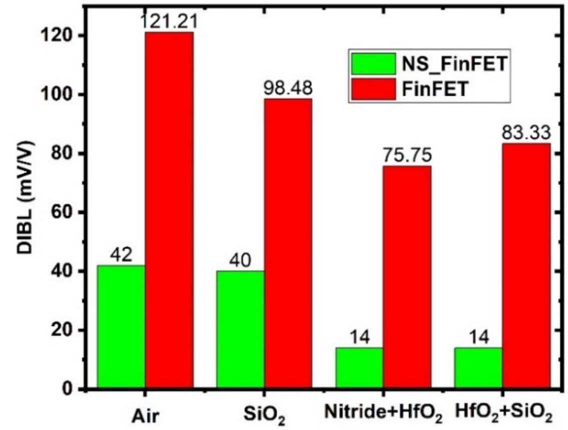

FIGURE 8. DIBL of NS-FET and FinFET for 10 nm technology node.

TABLE VI
SS FOR NS-FET AND FINFET WITH VARYING SPACER MATERIALS

Spaces Material	SS in NS-FET (mV/dec)	SS in FinFET (mV/dec)
Air	67	70.63
SiO_2	65	65.6
Nitride+HfO_2	62	62.01
HfO_2+SiO_2	61.2	62.86

V_{th1} at V_{DS1} = 0.75V (high drain voltage) and V_{th2} at V_{DS2} = 0.04V (low drain voltage) are vital parameters required while calculating the DIBL as indicated in (1). DIBL in case of FinFET with Air spacer (single-*k*) is measured to be 121.21 mV/V, and this value decreased by 65.34% to 42 mV/V in the case of NS-FET. Similarly, the DIBL value for FinFET with SiO_2 spacer (single-*k*) is 98.48 mV /V, decreasing by 59.37% to 40 mV/ V with NS-FET. For FinFET with Nitride+HfO_2 spacer layers (dual-*k*), the DIBL value is 75.75 mV/V, and it is decreased by 81.43% to 14 mV/V with NS-FET. Lastly, the DIBL value for FinFET with HfO_2+SiO_2 spacers (dual-k) is 83.33 mV/V, and it is decreased by 83.19% to 14 mV/V with NS-FET, as shown in Table V and Fig. 8.

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The subthreshold swing is a parameter claiming to improve when the short channel effects in the device are low [2]. The SS value obtained in NS-FET is 67 mV/dec witnessing an improvement of 5.28% compared to the single-*k* (air) FinFET. Compared to NS-FET, the SS has improved by 0.92% for the spacer material SiO_2. Likewise, as mentioned in Table VI and illustrated in Fig. 9, the SS for dual-*k* (Nitride+HfO_2) for either of the devices remained unaltered but displayed an improvement in SS compared to the former materials. Similar improvement can be seen in dual-*k* (HfO_2+SiO_2), where the SS almost meets its ideal value of 60mV/Dec [3]. The dielectric fringing fields reduce leakages as spacer materials change from air to low-*k* to high-*k*. This lowers the SCEs and thus enhances the device's SS and DIBL characteristics. NS-FET, built with the concept of multiple channels, gathers an advantage when compared to FinFET in improving the SS and DIBL.

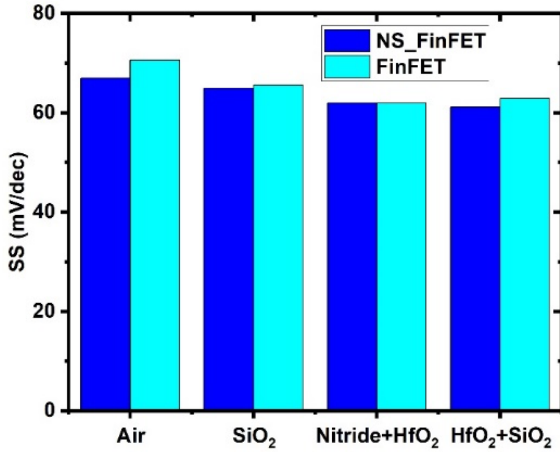

FIGURE 9. SS of NS-FET and FinFET for 10 nm technology.

TABLE VII
PERFORMANCE COMPARISON

Devices	V_{th} (V)	I_{ON}/I_{OFF} Ratio	SS in (mV/dec)	DIBL (mV/V)
NS-FET with spacers HfO_2+SiO_2	0.37	1.2E5	61.2	14
NS-FET with spacers Nitride+HfO_2	0.38	1.1E6	62	14
JL NS-FET [22]	0.38	3.54E7	63.7	51.55
INV NS-FET [23]	0.38	5.03E7	61.48	34.29
Multi-Channel-Multi-Gate-Based Junction-less FET [24]	0.86	9.6E12	61.51	22
Heterojunction $Si_{1-x}Ge_x$ FinFET [25]	0.86	4.5E12	58.67	52.37

Additionally, Table VII contrasts the DC characteristics of the proposed NS FETs with those of the Junction-less NSFET, the Heterojunction $Si_{1-x}Ge_x$ FinFET, and the Multi-Channel-Multi-Gate-Based Junction-less Field Effect Transistor that have been reported in the literature [22]– [25]. As Table VII makes abundantly evident, NS-FETs with different space charge region materials have comparable [22], [23], or much lower threshold voltages [24], [25], as well as reasonable SS and DIBL, all of which greatly reduce SCE and make them perfect for low power applications.

IV. POWER ANALYSIS

When determining if low power consumption will be attained, a device's power consumption measurement is essential. Thus, assuming V_{dd} = 0.7V and gate work function of 4.8 eV the following formula is used to compute the dynamic and average power [26], [28], [29]. The C_{OX} represents the equivalent oxide capacitance obtained by the series combination of capacitance due to spacer oxide layers [27]. The variation of capacitances with varying gate voltage is presented in Fig. 10. Upon multiplication of maximum C_{OX} with V_{dd}^2 and $0.5V_{dd}^2$, dynamic and average power are obtained as per (3) and (4), respectively.

$$Dynamic\ power = C_{ox}.V_{dd}^{\ 2} \tag{3}$$

$$Average\ Power = \frac{1}{2}C_{ox}.V_{dd}^{\ 2} \tag{4}$$

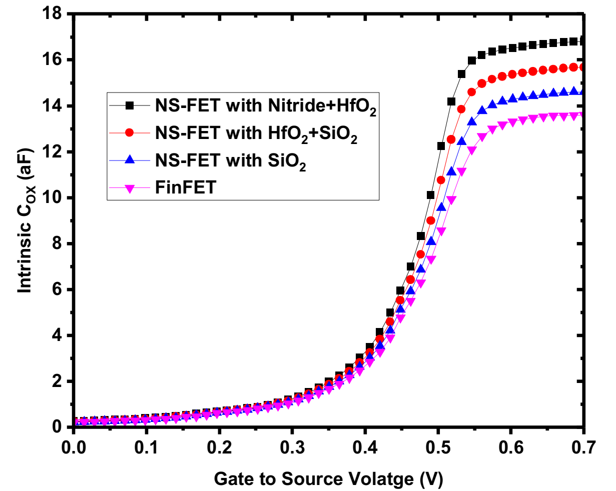

FIGURE 10 C_{OX}~V_{GS} Characteristics for FinFET vs NS-FET structures.

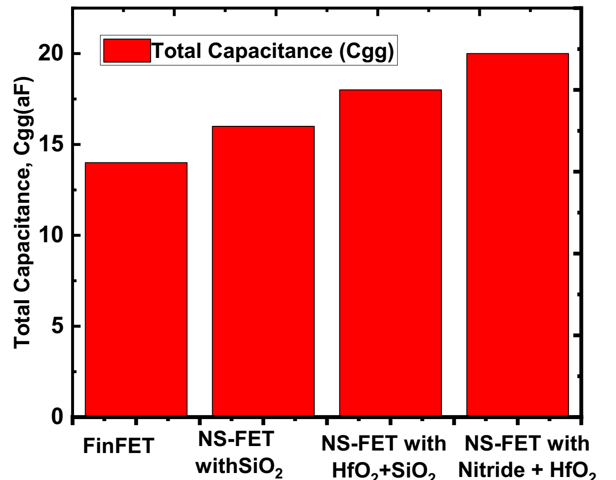

FIGURE 11 C_{OX}~V_{GS} Characteristics for FinFET vs NS-FET structures.

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Figure 11 depicts the total capacitance (Cgg=Cgs+Cgd) of various FETs. The rise in Cgs and Cgd results in rise in the total capacitance with increase in dielectric permittivity. Thus, Cgg is low for FinFET combination followed by SiO_2 and HfO_2+SiO2 and Nitride+HfO_2.

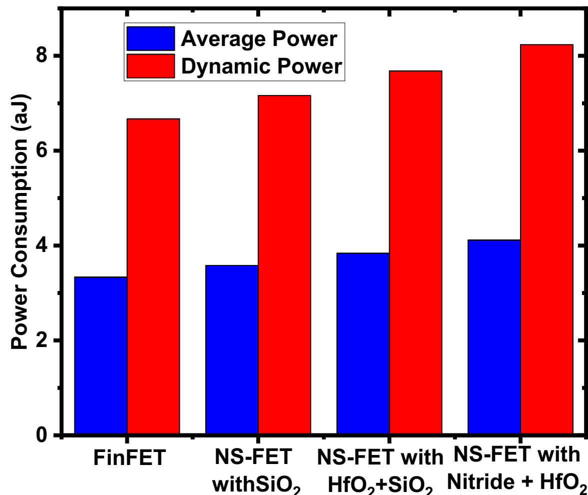
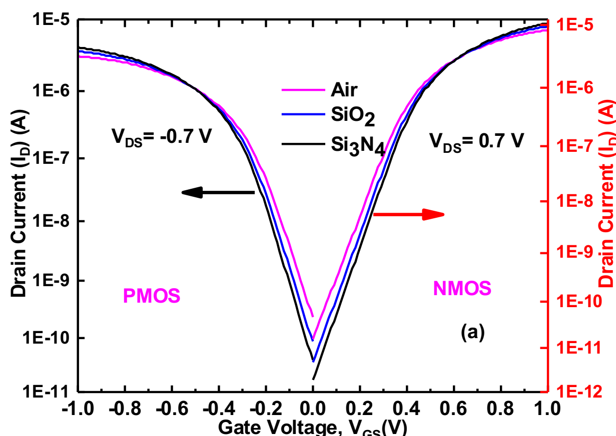


FIGURE 12 Power consumption in attoJoule for NS-FET.

The variation of dynamic and average power of FinFET, proposed NS-FET with single dielectric SiO_2 and with diverse space charge regions including HfO_2+SiO_2, and Nitride+HfO_2, are shown in Fig. 12. Compared to a traditional FinFET, the NS-FET with Nitride+HfO_2 as the space charge region consumes a relatively little amount of average and dynamic power.



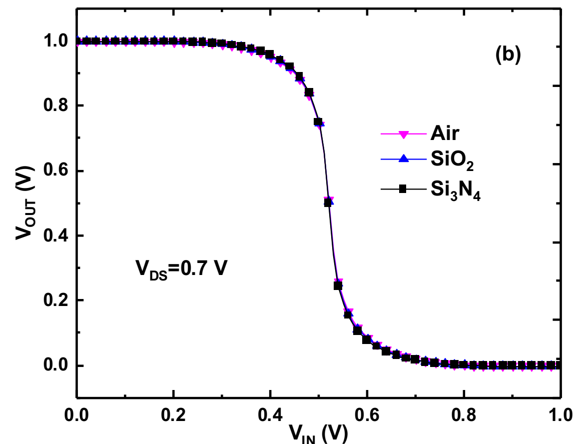


FIGURE 13 (a) Transfer characteristics for PMOS and NMOS inverters and (b) CMOS inverters.

V. CIRCUIT PERFORMANCE

The CADENCE tool is used to examine the device's efficiency towards the circuit for different spacer materials. The performance of the CMOS inverter is shown in Fig. 13. Fig. 13(a) displays the PMOS and NMOS transfer characteristics of the NS-FET at V_{DS} = 0.7V. The Si_3N_4's strong fringing fields cause it to have lower I_{OFF} and greater I_{ON}. The V_{OUT} with V_{IN} fluctuation is shown in Fig. 13(b). There are slight differences in the transfer characteristics between SiO_2, Air, and Si_3N_4 dielectrics.

VI. CONCLUSION

The developed 10 nm technology FINFET and NS-FET has two channels with uniform NS-FET doping concentrations for a variety of spacer region materials with single-k (Air and SiO_2), dual-k (HfO_2+SiO_2 and Nitride+HfO_2) spacers. The device is designed with GAA and FDSOI technology. The 3D devices are thoroughly investigated for factors such as transfer characteristics, threshold voltage, I_{ON} to I_{OFF} ratio, DIBL, and SS. In comparison to FinFET, the DIBL of the NS-FET's changing dielectric spacer materials like Air, SiO_2, HfO_2+SiO_2, and Nitride+HfO_2 is improved by 65.34%, 59.37%, 81.43%, and 83.19%, respectively, while the SS is decreased by 5.28%, 0.92%, 0.02%, and 2.68%. The I_{ON}/I_{OFF} ratio for a single-k spacer is better. From this result, it can be concluded that subthreshold leakage is decreasing for NS-FET in comparison to FinFET by changing the spacer materials. Furthermore, the power consumption is comparably very small for NS FET with diverse space charge regions. The leakage current reduction implies and assures improved device performance for low-power nanoscale applications.

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